Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1-2. **Cancelled**

3. **(Currently Amended)** A memory control apparatus in a computing system comprising:

a memory controller and a buffer;

said memory controller and buffer being connected by a bidirectional data bus and a control interface;

said buffer being connected to a random-access memory bus for read and write operations;

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory;

a second buffer serving as a tag buffer, said second buffer being connected to said random-access memory bus for read and write operations;

said second buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

and a data access and control bus connected between the tag buffer and the system memory to control read and write operations from and to system memory; and

~~The memory control apparatus of claim 2, further comprising:~~

a tag control input signal designating said second buffer as the tag buffer.

4. **(Original)** The memory control apparatus of claim 3, further comprising:

a memory interface tag bus between the memory controller and the second buffer.

5-6. **Cancelled**

7. **(Currently Amended)** A memory control apparatus in a computing system comprising:

a memory controller and a buffer;

said memory controller and buffer being connected by a bidirectional data bus and a control interface;

said buffer being connected to a random-access memory bus for read and write operations;

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller; and

a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory;

~~The memory control apparatus of claim 1,~~ wherein the buffer comprises:

a read data queue.

8. **(Currently Amended)** A memory control apparatus in a computing system comprising:

a memory controller and a buffer;

said memory controller and buffer being connected by a bidirectional data bus and a control interface;

said buffer being connected to a random-access memory bus for read and write operations;

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller; and

a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory;

~~The memory control apparatus of claim 1,~~ wherein the buffer comprises:

a write data queue.

9. **(Currently Amended)** A memory control apparatus in a computing system comprising:

a memory controller and a buffer;

said memory controller and buffer being connected by a bidirectional data bus and a control interface;

said buffer being connected to a random-access memory bus for read and write operations;

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller; and

a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory;

~~The memory control apparatus of claim 1,~~ wherein the buffer comprises:

a tag data queue.

10-16. **Cancelled**

17. **(Currently Amended)** A method for data transfer between a memory controller and a system memory bus connected to system memory in a computing system comprising:

interposing a buffer between said system memory bus and the memory controller;

providing to said buffer memory interface addresses and memory interface control commands to facilitate said buffer's read and write operations from and to said system memory;

addressing said system memory through said buffer to accomplish read and write operations between the system memory and the memory controller;

decoding in said buffer the memory interface control commands;

temporarily storing data read and write memory data in the buffer during data transfer between the system memory and the buffer;

transferring read and write memory data between said memory controller and said buffer during read and write operations; and

~~The method of claim 12, further comprising:~~

interleaving read and write operations in sequences of memory operations between the controller and multiple independent portions of system memory through the buffer.

18. **Cancelled**